MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2016/2017

EEE1046 – ELECTRONICS III

(All sections / Groups)

26 MAY 2017
3:00 PM – 5:00 PM
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 6 pages (including the cover page) with 4 Questions only.

2. Attempt **ALL** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please write all your answers in the Answer Booklet provided.

Question 1

(a) An ideal non-inverting amplifier consists of an operational amplifier (op-amp) and an external negative feedback circuit.

(i) Explain the term *negative feedback*. Next, state the **TWO** fundamental rules that are applied in the analysis of an ideal op-amp. [2+2 marks]

(ii) Sketch the schematic diagram of an ideal non-inverting op-amp circuit. Label the series input resistor R_1, feedback resistor R_F, input voltage V_i, and output voltage V_o accordingly. [3 marks]

(iii) With the aid of the sketch in Part (a) (ii), derive the equation for the closed loop voltage gain of the ideal non-inverting amplifier. [4 marks]

(b) Figure Q1 (b) (i) depicts the schematic diagram of an ideal op-amp differentiator circuit. An input signal with a waveform as shown in Figure Q1 (b) (ii) is applied to the differentiator.

(i) Derive the expression for the output voltage V_o of the ideal differentiator. [4 marks]

(ii) The differentiator has C_1 = 120 pF and R_F = 33 kΩ. Determine the output voltage and draw the graph of the output waveform relative to the input signal. [7 marks]

(iii) At high frequencies, the ideal differentiator is susceptible to electrical noise. Explain why. [3 marks]

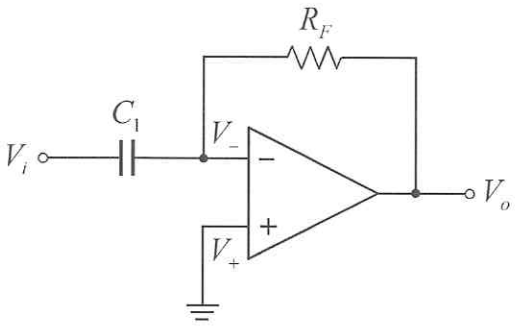

Figure Q1 (b) (i)

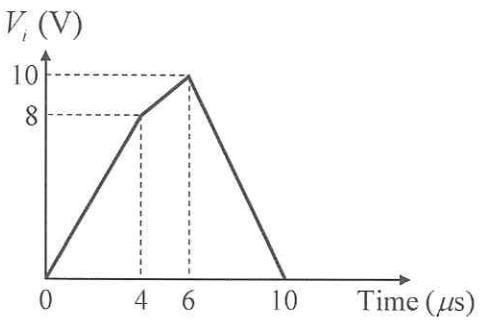

Figure Q1 (b) (ii)

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Question 2

(a) The total output voltage gain of an op-amp is due to its differential signal and common signal at the input. Given an op-amp which its output voltage V_0 is 1.002 V when $V_+ = 501$ μV and $V_- = 499$ μV. When $V_+ = 606$ μV and $V_- = 604$ μV, V_0 is 1.00201 V. Calculate the common mode gain A_{CM}, open loop gain A_{OL} and common-mode rejection ratio (in decibels) of the amplifier. [10 marks]

(b) Describe the terms;

(i) Input bias current, I_{BIAS}. [2 marks]

(ii) Power Supply Rejection Ratio (PSRR). [2 marks]

(c) Internal stages of op-amp circuit contribute to its own critical frequency at each stage. Given an op-amp with two critical frequencies, which are $f_{c1} = 10$ kHz and $f_{c2} = 50$ kHz.

(i) Calculate the total phase-lag at frequency, $f = 30$ kHz and 80 kHz. [5 marks]

(ii) If 30 kHz is the unity-gain bandwidth of the op-amp, find its phase margin. Is this op-amp stable? [3 marks]

(iii) If the op-amp is used to form an inverting amplifier with voltage gain equal to -8. Find the required value for input resistor, R_1 if feedback resistor, $R_F = 25$ kΩ. [3 marks]

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Question 3

(a) The voltage from an unregulated power supply may vary from 12 V_{FL} (at full load) to 16 V_{NL} (at no load). A power transistor with a maximum rating of 1 A is to be used as the pass transistor of a 9 V regulator. The minimum h_{FE} of the transistor is 25. The required maximum load current, I_L is 500 mA. Also given that the Zener knee current, I_{ZK} is 10 mA and the base-emitter voltage, V_{BE} of the transistor is 0.7 V.

(i) Sketch the series voltage regulator circuit. With the aid of the sketch, design the circuit by computing the value of R. [10 marks]

(ii) Determine the power dissipation of the pass transistor. [2 marks]

(b) Determine the regulated voltage, V_L and circuit currents, I_L, I_S and I_C for the shunt regulator shown in Figure Q3 (b). Given the value of the regulator V_i = 22 V, V_Z = 8.2 V, R_L = 100 Ω, and R_S = 120 Ω. [7 marks]

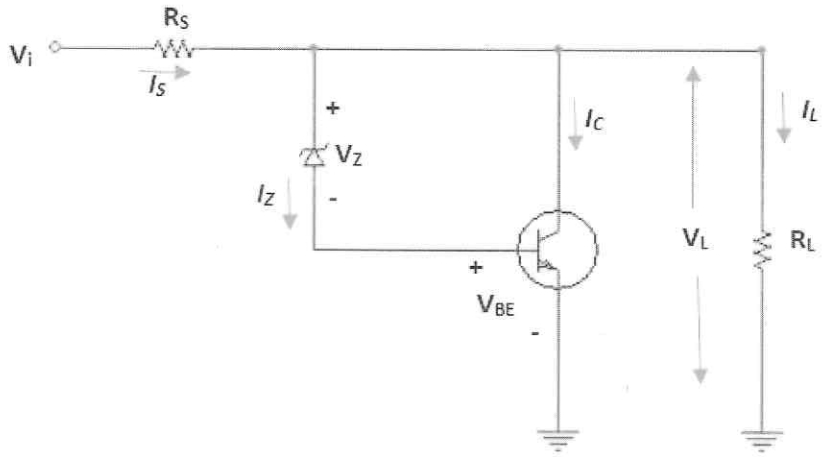

Figure Q3 (b)

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(c) A Colpitts oscillator is shown in Figure Q3 (c). If the value of capacitors are C_1 = 0.1 μF and C_2 = 0.01 μF, and the value of inductor L is 50 mH,

(i) Determine the frequency for the oscillator. Assume there is negligible loading on the feedback circuit and the Q is greater than 10. [4 marks]

(ii) Find the frequency if the oscillator is loaded to a point where the Q drops to 8. [2 marks]

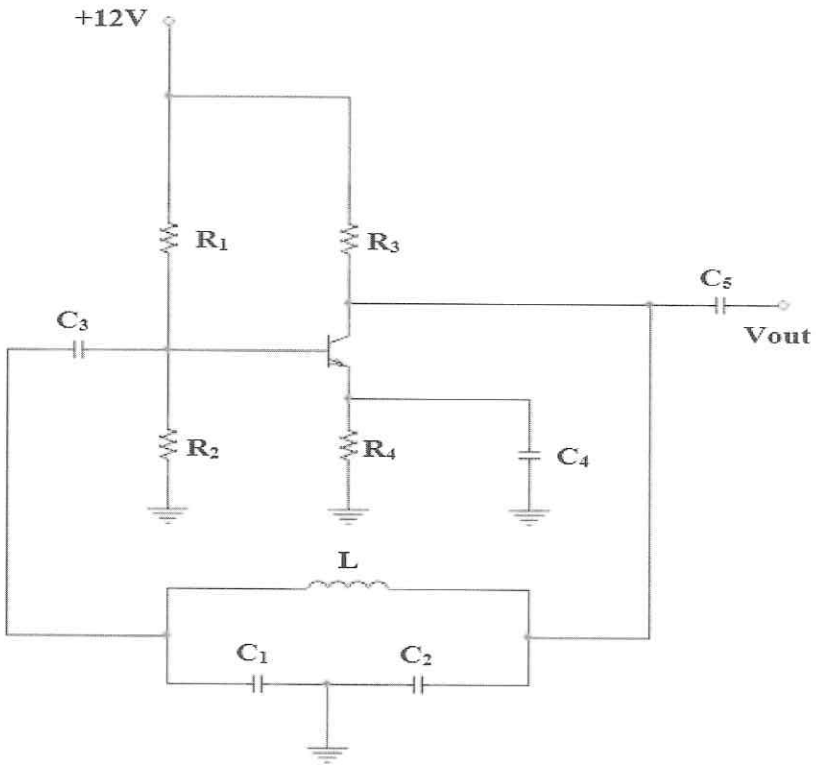

Figure Q3 (c)

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Question 4

(a) A band reject filter with a band of zero-gain for f_c = 3 kHz. BW = 1 kHz and K_{PB} = 2 is constructed of a first order Low-Pass Filter (1st Order LP) and a first order High-Pass Filter (1st Order HP). Calculate,

(i) f_L and f_H . [6 marks]
(ii) R (for f_L)and R' (for f_H). [6 marks]

(Given $K_{PB} = K_{HP} = K_{LP} = 2$, $C = 5$ nF, $C' = 10$ nF, $R_F = R_1 = R_1' = R_2 = R_3 = R_4 = 10$ kΩ)

b) Draw the schematic of a precision rectifier (super diode). The circuit must consist of the following item. (One op-amp, one diode, one resistor, one AC supply). [7 marks]

c) With reference to Figure Q4 (a). Given $+V_{out(max)} = +12$V, $-V_{out(max)} = -6$V, $R_1 = 22$ kΩ, $R_2 = 22$ kΩ. Calculate:

(i) Upper trigger level, V_{UTP} [3 marks]

(ii) Lower trigger level, V_{LTP} [3 marks]

End of paper

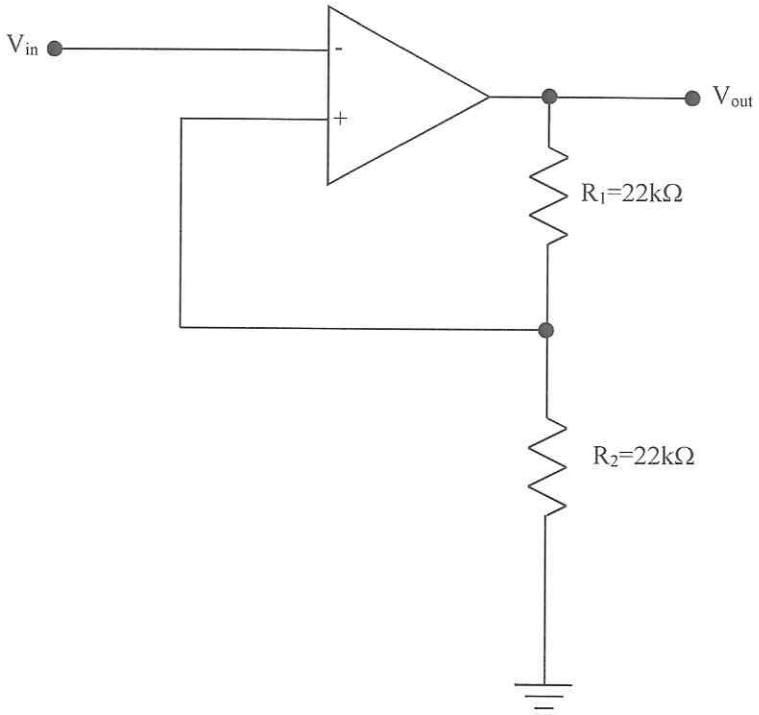

Figure Q4(a)